深圳市微而盛科技有限公司
Shenzhen Wei Er Sheng Technology CO.,Ltd.

TFT-LCD MODULE SPECIFITION
FOR APPROVAL

CUSTOMER MODEL NO. WES101GBI-003

FX MODEL NO :

ALL MATERIAL AGREE WITH RoHS

FOR CUSTOMER APPROVAL	SUPPLIER SIGNATURE
APPROVED BY :	APPROVED BY :
REVIEEDE BY :	REVIEEDE BY :
PEREPARED BY :	PEREPARED BY :
APPROVAL DATE:	MAKE DATE:

Revision Notice	Description	Page	Rev. Date
0.0	First revision (Tentative)	--	2019/06/04

TABLE OF CONTENTS

1. GENERAL DESCRIPTION

1.1 DESCRIPTION

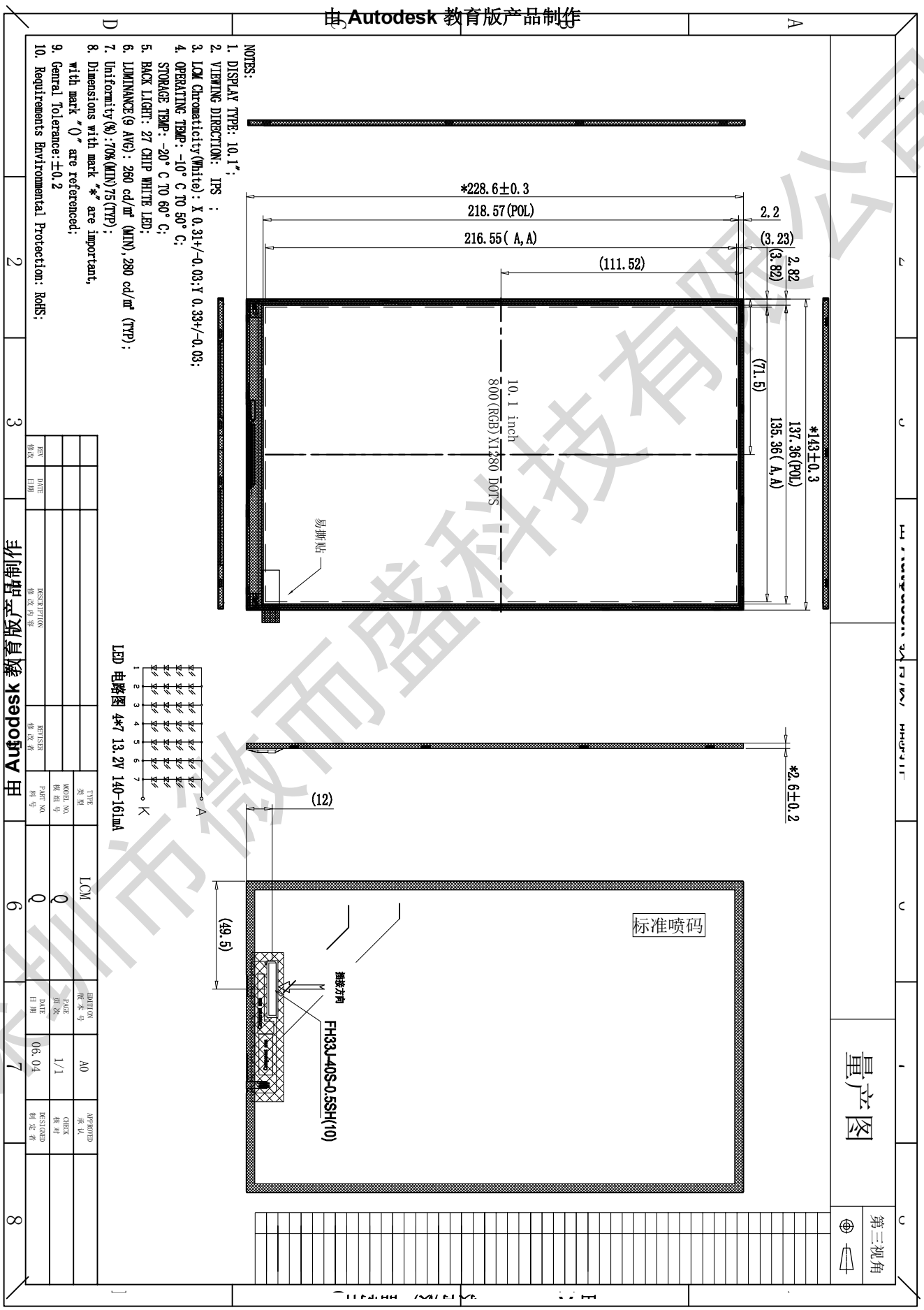
WES101GBI-003 ***is a color active matrix thin film tr*** ansistor (TFT) IPS liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. It is composed of a TFT LCD panel, Driver IC ,FPC and Backlight.

1.2 FEATURES:

No.	Item	Specification	Unit
1	Panel Size	10.1”	inch
2	Number of Pixels	800 x3(RGB) x 1280	pixels
3	Active Area	135.360(W)x216.576(H)	mm
4	Pixel Pitch	0. 1692 x 0.1692	mm
5	OutlineDimension	228.6(W) x 143(H) x2.60(D) mm	
6	Number of Colors	16.7M	-
7	Display Mode	Normally Black	-
8	ViewingDirection	IPS	
9	Pixel Arrangement	RGB vertical stripe	-
10	Luminance (cd/m^2)	260(TYP.)	nit
11	Contrast Ratio	1000(TYP.)	
12	Surface Treatment	Anti-glare	-
13	Interface	MIPI	-
14	Backlight	White LED	-
15	Operation Temperature	-10~50	℃
16	Storage Temperature	-20~60	℃
17	Weight	TPD	g

2. MECHANICAL SPECIFICATION

NOTES:
1. DISPLAY TYPE: 10.1";
2. VIEWING DIRECTION: IPS ;
3. LCM Chromaticity(White): X 0.31+/-0.03;Y 0.33+/-0.03;
4. OPERATING TEMP: -10° C TO 50° C;
   STORAGE TEMP: -20° C TO 60° C;
5. BACK LIGHT: 27 CHIP WHITE LED;
6. LUMINANCE(9 AVG): 260 cd/㎡ (MIN),280 cd/㎡ (TYP);
7. Uniformity(%):70%(MIN)75(TYP);
8. Dimensions with mark "*" are important,
   with mark "()" are referenced;
9. Genral Tolerance:±0.2
10. Requirements Environmental Protection: RoHS;



3. PIN DESCRIPTION

PIN NO.	Symbol	Description
1	NC	No connection
2	VDD	Power Voltage for digital circuit 3.3V
3	VCCIO	Power Voltage for digital circuit 1.8V Note 1
4	GND	Ground
5	Reset	Global reset pin 1.8V Note 1
6	NC	No connection
7	GND	Ground
8	MIPI_0N	-MIPI differential data input
9	MIPI_0P	+MIPI differential data input
10	GND	Ground
11	MIPI_1N	-MIPI differential data input
12	MIPI_1P	+MIPI differential data input
13	GND	Ground
14	MIPI_CKN	-MIPI differential clock input
15	MIPI_CKP	+MIPI differential clock input
16	GND	Ground
17	MIPI_2N	-MIPI differential data input
18	MIPI_2P	+MIPI differential data input
19	GND	Ground
20	MIPI_3N	-MIPI differential data input
21	MIPI_3P	+MIPI differential data input
22	GND	Ground
23	NC	No connection
24	NC	No connection
25	GND	Ground
26	ID	
27	PWMO	PWM control signal for LED driver(CABC)
28	NC	No connection
29	NC	No connection
30	GND	Ground

31	LED-	LED Cathode
32	LED-	LED Cathode
33	NC	No connection
34	NC	No connection
35	NC	No connection
36	NC	No connection
37	NC	No connection
38	NC	No connection
39	LED+	LED Anode
40	LED+	LED Anode

Note 1： The 3PIN and 5PIN should be the same as 1.8v or 3.3v

4. Absolute Max. Rating

Item	Symbol	Values		Unit
		Min.	Max.	
Power Voltage	VDD	-0.3	+5.0	V
Backlight forward current	I_{LED}	0	25	mA(For each LED)
Input Signal Voltage	V_I	-0.3	VCC	V
Operation Temperature	T_{OP}	-10	50	℃
Storage Temperature	T_{ST}	-20	60	℃

4.1 Typical Operation Conditions

Item	Symbol	Values			Unit
		Min.	Typ.	Max.	
Power Voltage	VDD	3.0	3.3	3.6	V
Current Consumption	I_{VCC}	-	--	TBD	mA
	I_{LED}	--	140	160	mA

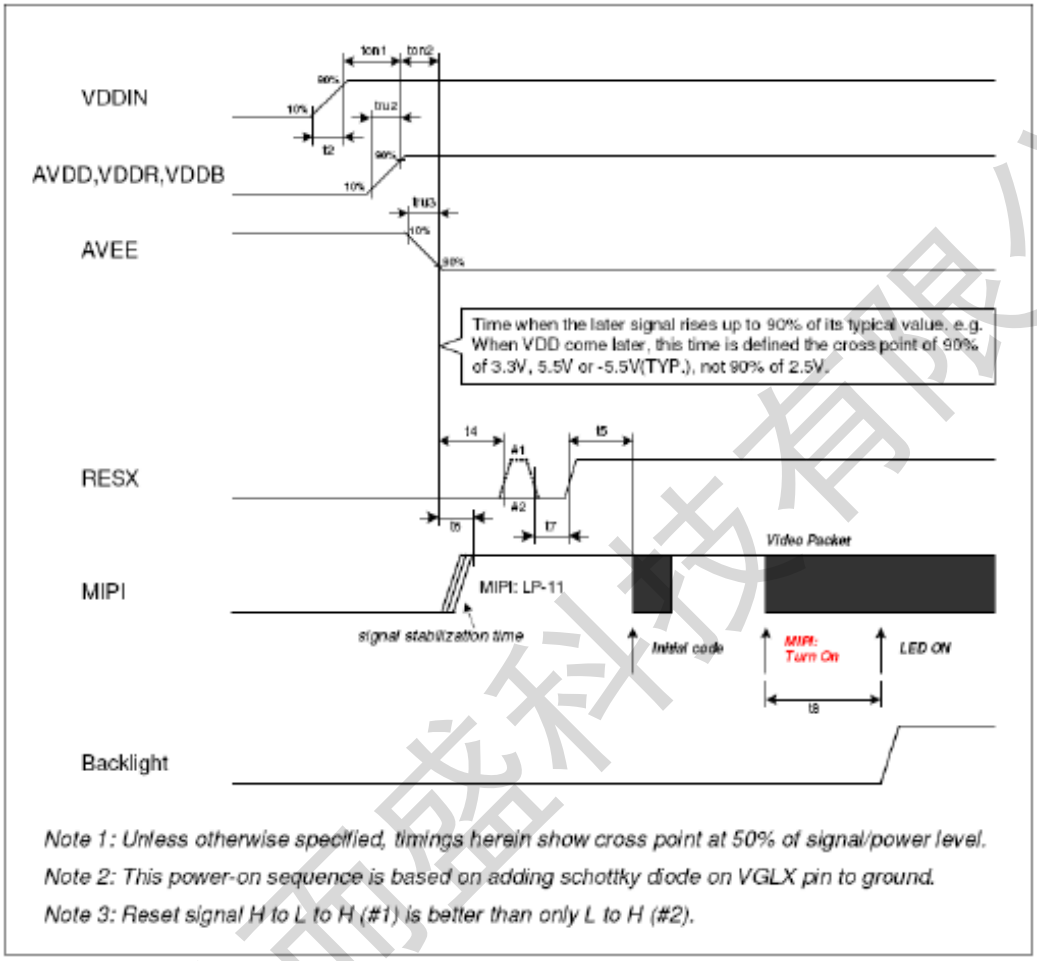
4.2 LED Back Light Specifi cation (21 White Chips)

Item	Symbol	Condition	Min	Typ	Max	Unit
Forward Voltage	Vf	If=140mA	11.2	-	13.2	V
Uniformity (with L/G)	ΔB_p	If=140mA	70	75	-	%
Luminance for LCM	/	If=140mA	----	280	-	cd/m^2

LED circuit:

5. Signal timing diagramPower Sequence

5.1 Power on



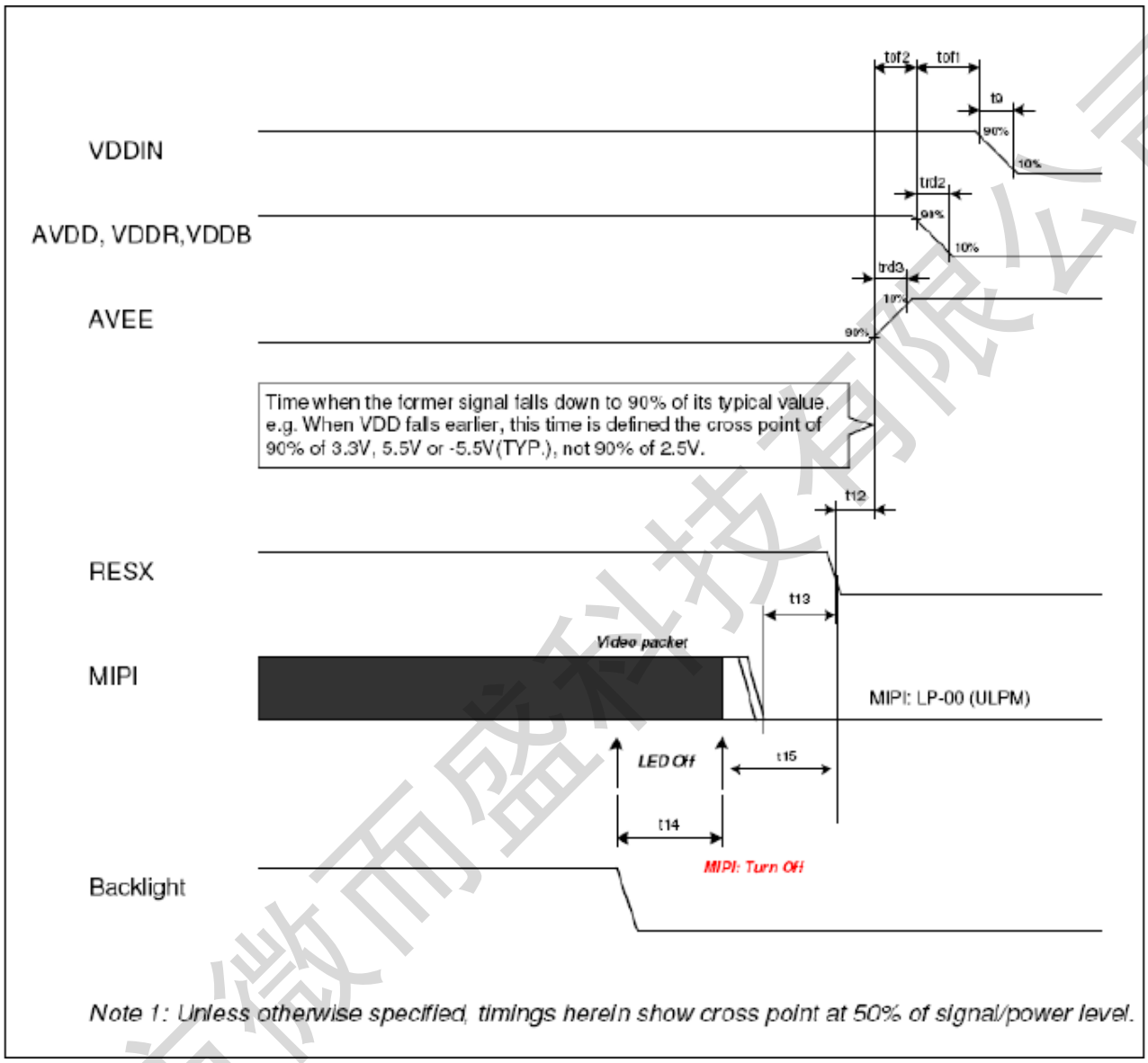
Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Note 2: This power-on sequence is based on adding schottky diode on VGLX pin to ground.

Note 3: Reset signal H to L to H (#1) is better than only L to H (#2).

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
ton1		No limit		ms	
ton2		0(Note)		ms	
ton3		No limit	-	ms	
ton4		No limit	-	ms	
t2			150	µs	
tru1			150	µs	
tru2			150	µs	
tru3			150	µs	
tru4			150	µs	
t4	40	-	-	ms	
t5	120			ms	
t6	0			ms	
t7	10			µs	
t8	8			VS	Keep data more than 8 frames (VS)

5.2 Power off



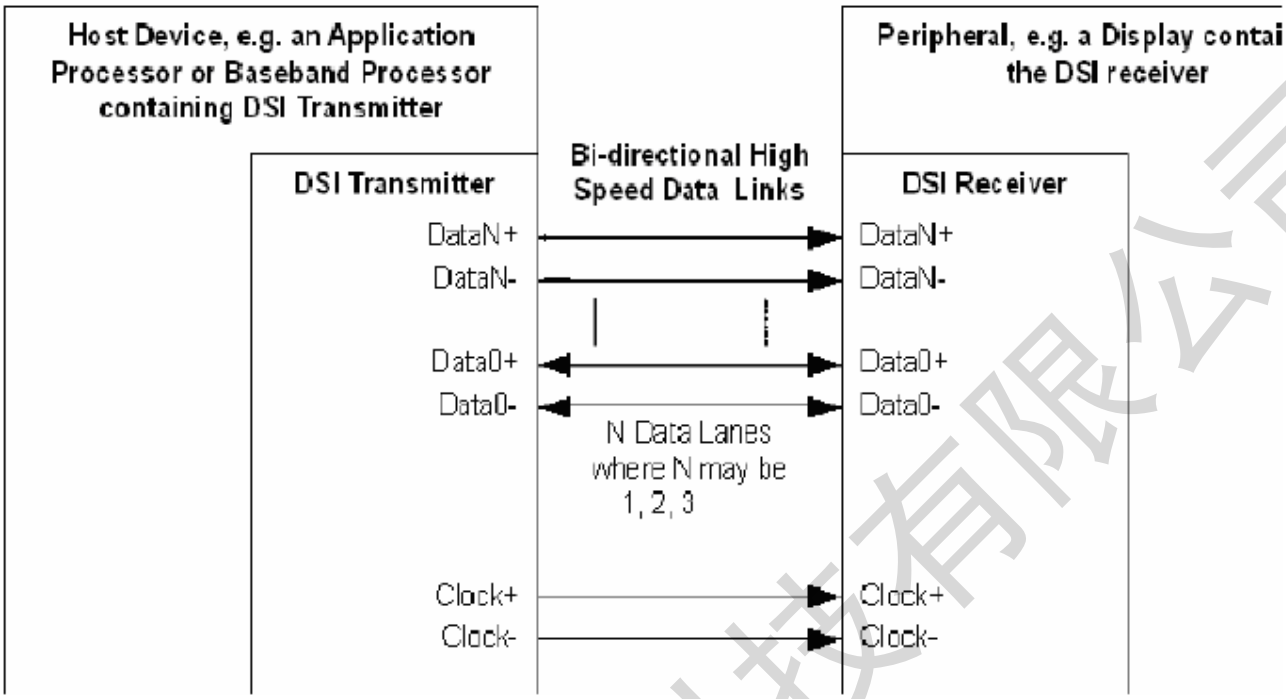
Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
t9	150			μs	
tof1		No limit		ms	
tof2		0(Note)	-	ms	
tof3		No limit	-	ms	
tof4		No limit		ms	
trd1	150			μs	
trd2	150			μs	
trd3	150			μs	
trd4	150			μs	
t12	0		-	ms	
t13	0			ms	
T14	0			ms	
T15	10			ms	

5.3 MIPI Timing characteristics

5.4 MIPI Lane Configuration

	MCU (Master) Display Module (Slave)
Clock Lane+/-	Unidirectional Lane ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane0+/-	Bi-directional Lane ■ Forward High-Speed ■ Bi-directional Escape Mode ■ Bi-directional LPDT
Data Lane1+/-	Unidirectional ■ Forward High speed
Data Lane2+/-	Unidirectional ■ Forward High speed
Data Lane3+/-	Unidirectional ■ Forward High speed

The connection between host device and display module is as reference.



6. MIPI AC Electrical characteristics

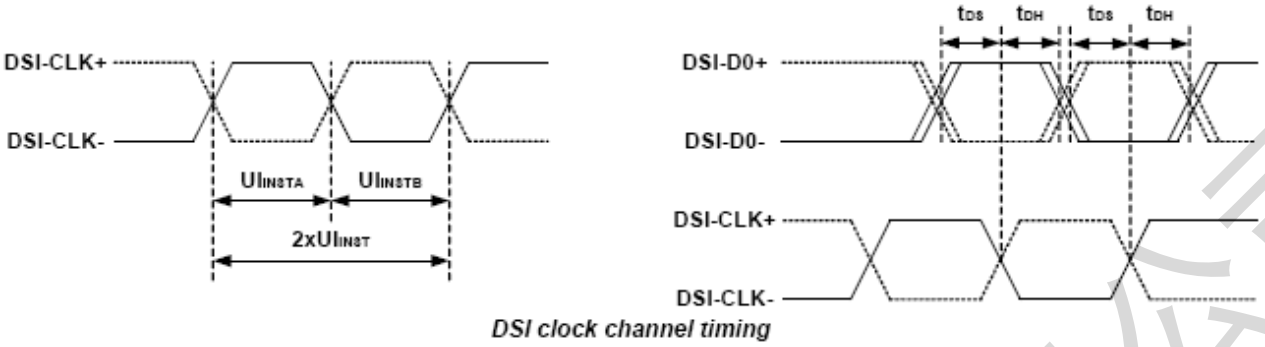
6.1 High Speed Transmission

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-CLK+/-	2xUI$_{INST}$	Double UI instantaneous	4	-	8	ns	4 Lane (Note 2)
			3	-	8	ns	3 Lane (Note 2)
			2.352	-	8	ns	2 Lane (Note 3)
DSI-CLK+/-	UI$_{INSTA}$ UI$_{INSTB}$	UI instantaneous halfs (UI = UI$_{INSTA}$ = UI$_{INSTB}$)	2	-	4	ns	4 Lane (Note 2)
			1.5	-	4	ns	3 Lane (Note 2)
			1.176	-	4	ns	2 Lane (Note 3)
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15xUI	-	-	ps	
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15xUI	-	-	ps	
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3xUI	ps	
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3xUI	ps	

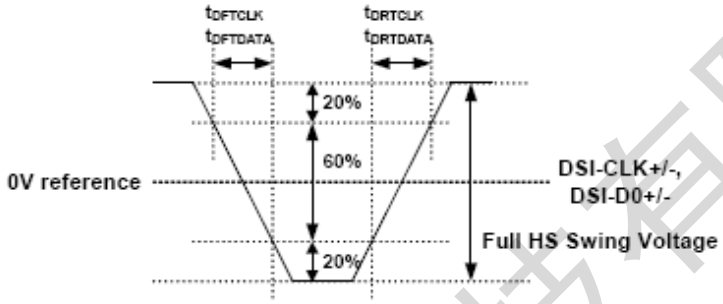
Note 1) Dn = D0, D1, D2 and D3.

Note 2) Maximum total bit rate is 2Gbps for 24-bit data format, 1.5Gbps for 18-bit data format and 1.33Gbps for 16-bit data format in 3 lanes or 4 lanes application which support to 800RGBx 1280 resolution.

Note 3) Maximum total bit rate is 1.7Gbps for 24-bit data format, 1.275Gbps for 18-bit data format and 1.13Gbps for 16-bit data format in 2 lanes application which support to 720RGBx1280 resolution.



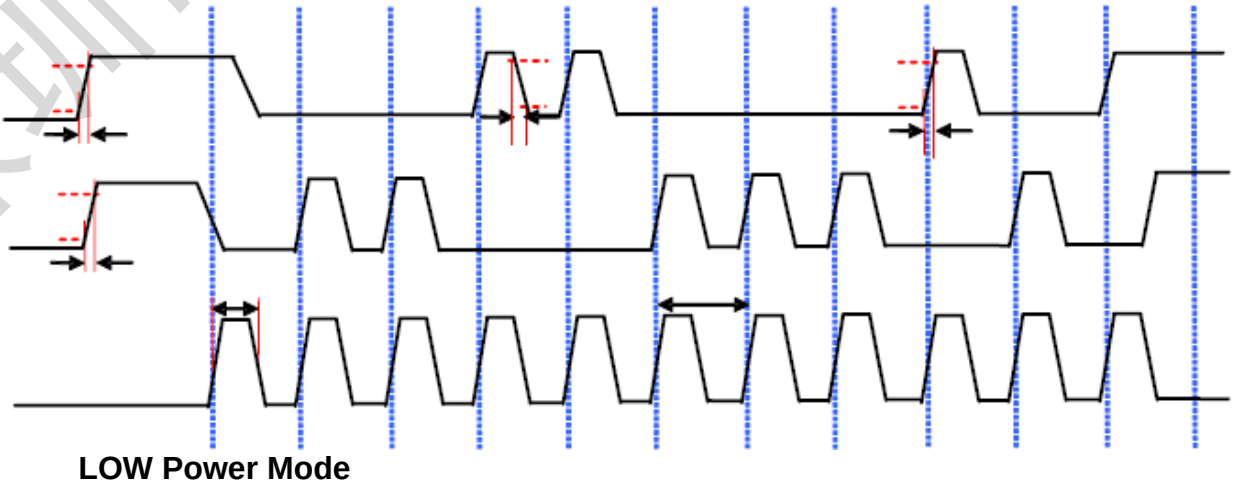
DSI clock channel timing



Rising and fall time on clock and data channel

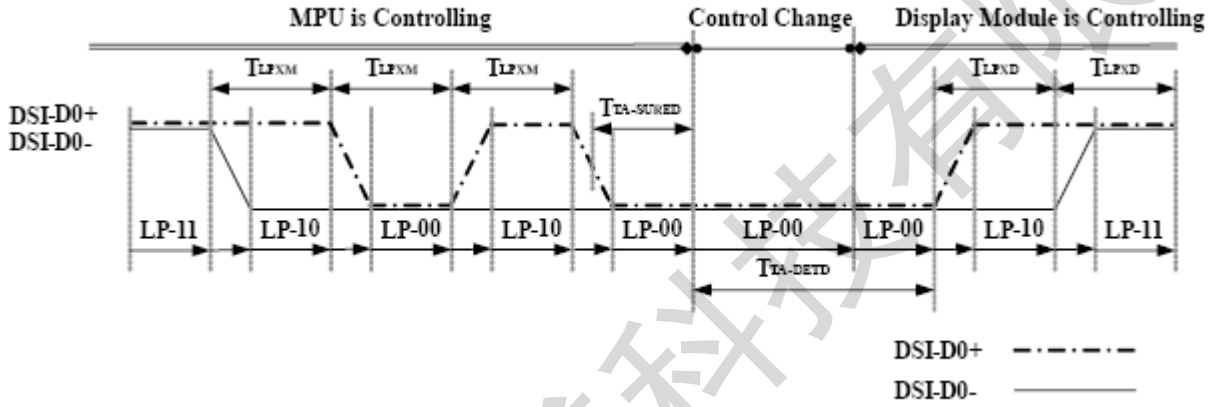
6.2 LP Transmission

Parameter	Symbol	Values			Unit	Remark
		Min.	Typ.	Max.		
DSI CLK frequency(LP)	F_{DSICLK_LP}			10	MHz	
DSI CLK Cycle Time(LP)	t_{CLKC_LP}	100			ns	
DSI Data Transfer Rate(LP)	t_{DSIR_LP}			10	Mbps	
15%-85% rise time and fall time	T_{RLP} / T_{FLP}	-	-	35	ns	
30%-85% rise time(from HS to LP)	T_{REOT}	-	-	35	ns	
Pulse width of the LP exclusive-OR clock	$t_{LP-PULSE-TX}$	50	65	-	ns	
Period of the LP exclusive-OR clock	$t_{LP-PRE-TX}$	100	130	-	ns	

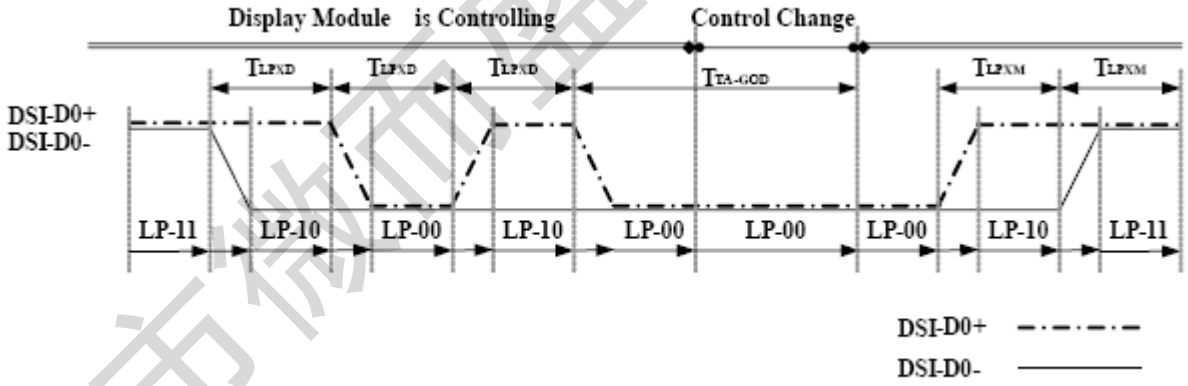


LOW Power Mode

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module	50	-	75	ns	Input
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU	50	-	75	ns	Output
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by display module	$5xT_{LPXD}$	-	-	ns	Input
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	$4xT_{LPXD}$	-	-	ns	Output



Bus Turnaround (BAT) from MPU to display module Timing



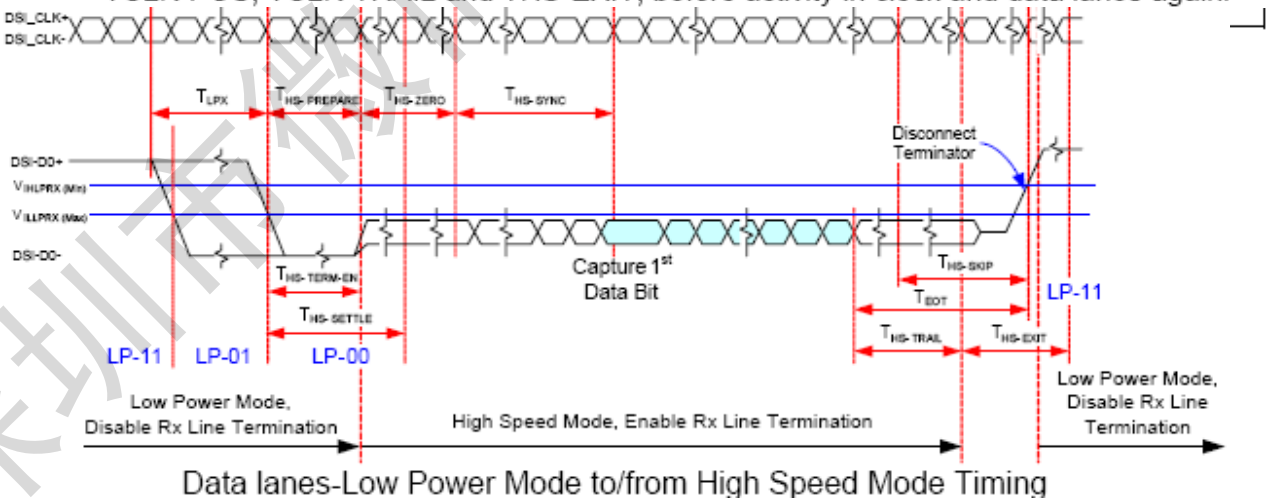
Bus Turnaround (BAT) from display module to MPU Timing

6.3 DSI Bursts

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	T_{LPX}	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Input
DSI-Dn+/-	$T_{HS-TERM-EN}$	Time to enable data receiver line termination measured from when Dn crosses V_{ILMAX}	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4xUI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI-CLK+/-	$T_{CLK-POS}$	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+52xUI	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input

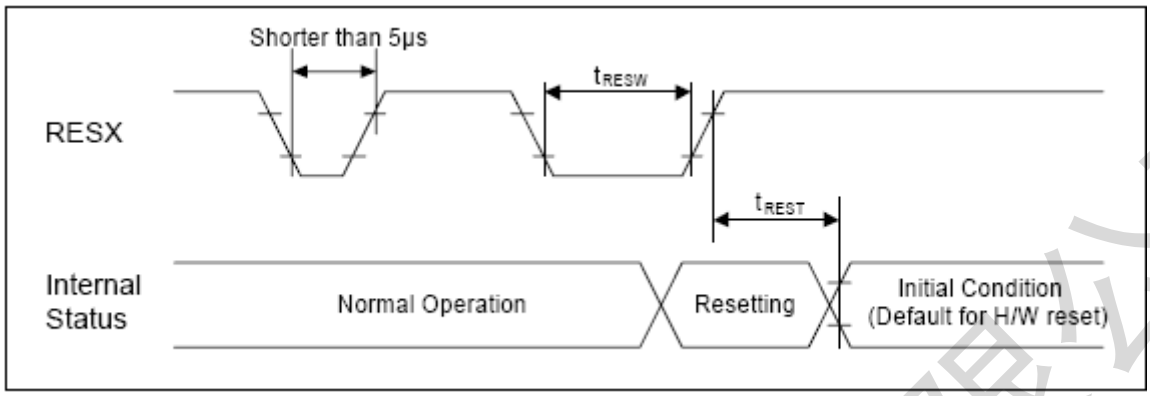
Note 1) Dn = D0, D1, D2 and D3.

Note 2) Two HS transmission can be sent with a break as short as THS-EXIT from each other in continuous clock mode. In discontinuous mode, the break is longer which account TCLK-POS, TCLK-TRAIL and THS-EXIT, before activity in clock and data lanes again.



Data lanes-Low Power Mode to/from High Speed Mode Timing

6.4 Reset Input Timing



Reset input timing

*(VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V,*Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	t_{RESW}	Reset "L" pulse width (Note 1)	10	-	-	µs	
	t_{REST}	Reset complete time (Note 2)	-	-	5	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode and Note 5

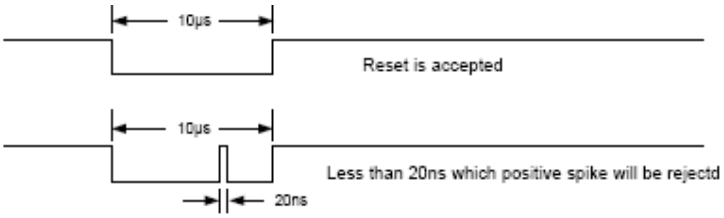
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5µs and 10µs	Reset Start

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.

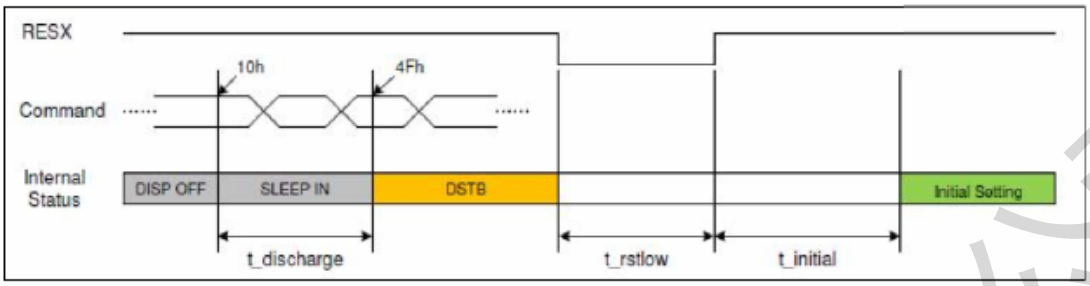
Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4) Spike Rejection also applies during a valid reset pulse as shown below:



Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

6.5 Deep Standby Mode Timing



(*VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V,*Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	$t_{discharge}$	Sleep in into DSTB delay time	-	-	100	ms	
	t_{rstlow}	Reset low pulse	3	-	-	ms	
	$t_{initial}$	Reset high to initial setting delay time	-	-	120	ms	

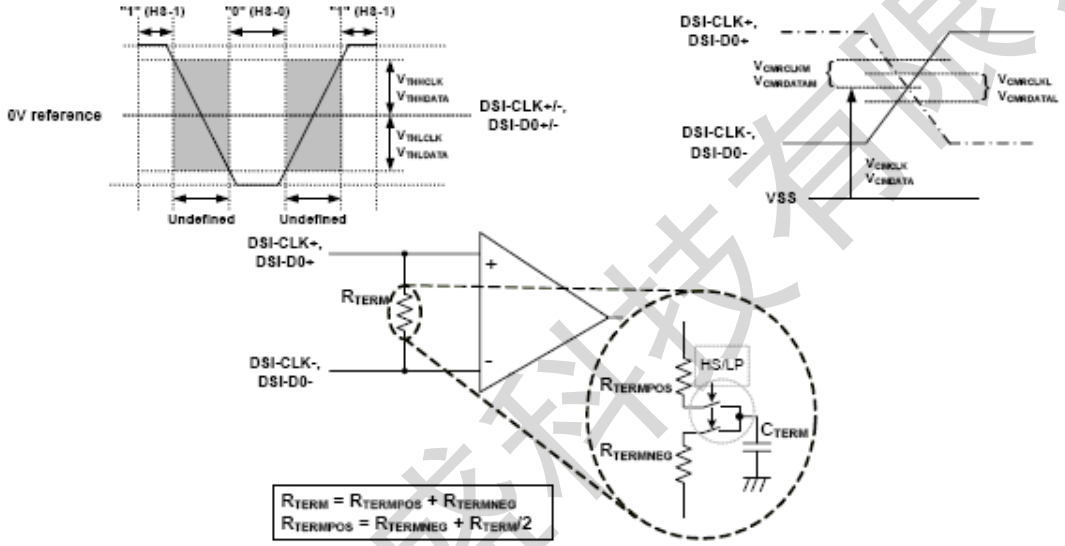
Note 1) t_discharge suggested delay time over 100ms.
Note 2) t_initial suggested delay time over 120ms..

6.6 DC Characteristics for DSI HS Mode

Parameter	Symbol	Conditions	Specification MIN	TYP	MAX	UNIT
Input voltage common mode range	V_{CMCLK} V_{CMDATA}	DSI-CLK+/-, DSI-Dn+/- (Note2, 3)	70	-	330	mV
Input voltage common mode variation (≤ 450MHz)	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI-CLK+/-, DSI-Dn+/- (Note 4)	-50	-	50	mV
Input voltage common mode variation (≥ 450MHz)	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI-CLK+/-, DSI-Dn+/-	-	-	100	mV
Low-level differential input voltage threshold	V_{THLCLK} $V_{THLDATA}$	DSI-CLK+/-, DSI-Dn+/-	-70	-	-	mV
High-level differential input voltage threshold	V_{THHCLK} $V_{THHDATA}$	DSI-CLK+/-, DSI-Dn+/-	-	-	70	mV
Single-ended input low voltage	V_{ILHS}	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	460	mV

Differential input termination resistor	R_{TERM}	DSI-CLK+/-, DSI-Dn+/-	80	100	125	Ω
Single-ended threshold voltage for termination enable	$V_{TERM-EN}$	DSI-CLK+/-, DSI-Dn+/-	-	-	450	mV
Termination capacitor	C_{TERM}	DSI-CLK+/-, DSI-Dn+/-	-	-	14	pF

Note 1) VDDI=1.7~1.9V, VCI=3.0 to 3.6V, GND=0V, Ta=-30 to 70 ºC (to +85 ºC no damage).
Note 2) Includes 50mV (-50mV to 50mV) ground difference.
Note 3) Without VCMRCLKM / VCMRDATAM .
Note 4) Without 50mV (-50mV to 50mV) ground difference.
Note 5) Dn=D0, D1, D2 and D3.



Differential voltage range, termination resistor and Common mode voltage

7. Optical Specifications

Item	Symbol	Condition	Values			Unit	Remark
			Min.	Typ.	Max.		
Viewing angle (CR≥ 10)	θ_L	Φ=180° (9 o'clock)	-	80	-	degree	Note 1
	θ_R	Φ=0°(3 o'clock)	-	80	-		
	θ_T	Φ=90° (12 o'clock)	-	80	-		
	θ_B	Φ=270° (6 o'clock)	-	80	-		
Response time Rise+Fall	T_{RT}	Normal θ=Φ=0°	-	20	30	msec	Note 3
Contrast ratio	CR		800	1000	-	-	Note 4
Color chromaticity	W_X		0.272	0.302	0.332	-	Note 2
	W_Y		0.291	0.321	0.351	-	Note 5 Note 6
Luminance	L		260	280	-	-	Note 6
Luminance uniformity	Y_U		70	75	-	%	Note 6,7

Note 1: Definition of viewing angle range

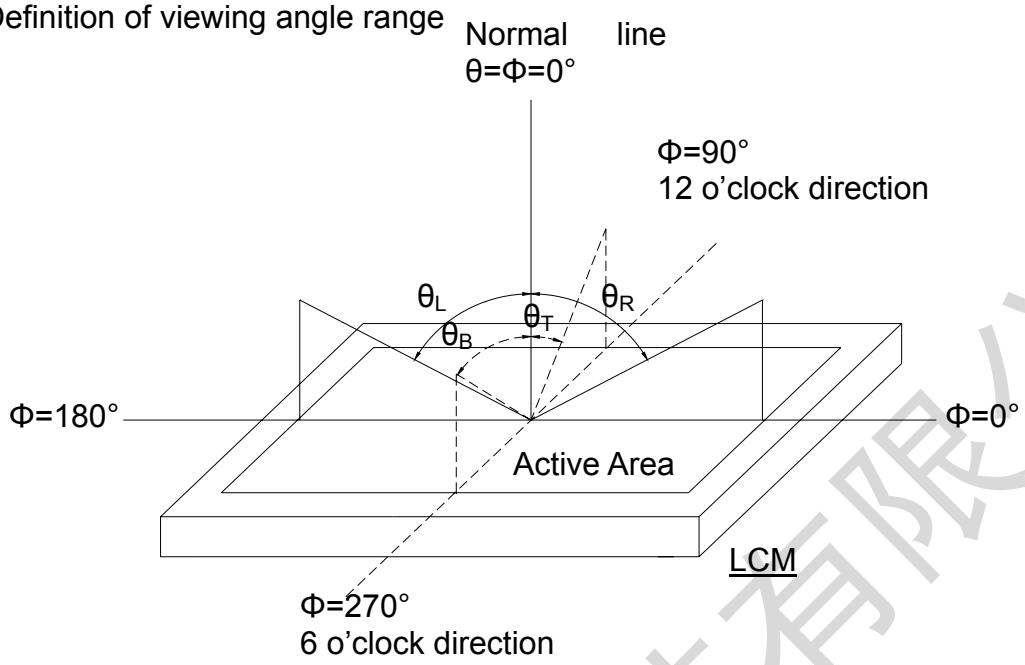


Fig. 4-1 Definition of viewing angle

Note 2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 30 minutes operation, the optical properties are measured at the center point of the LCD screen. (Viewing angle is measured by ELDIM-EZ contrast/Height :1.2mm ,Response time is measured by Photo detector TOPCON BM-5A, other items are measured by BM-7A/Field of view: 1° /Height: 500mm.)

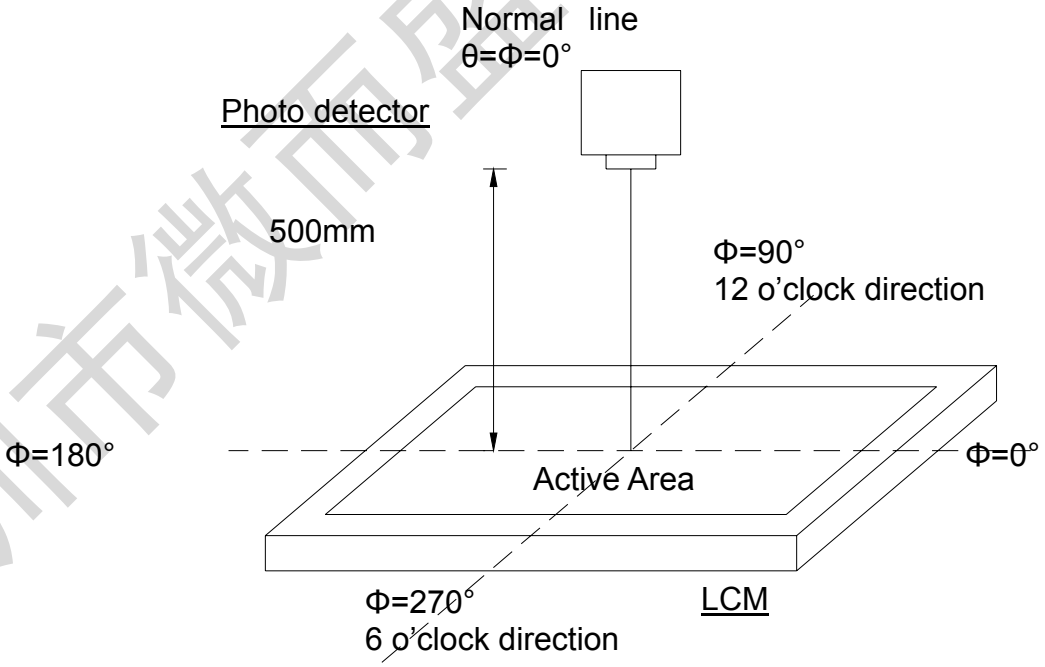


Fig. 4-2 Optical measurement system setup

Note 3: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo

detector output intensity changed from 10% to 90%.

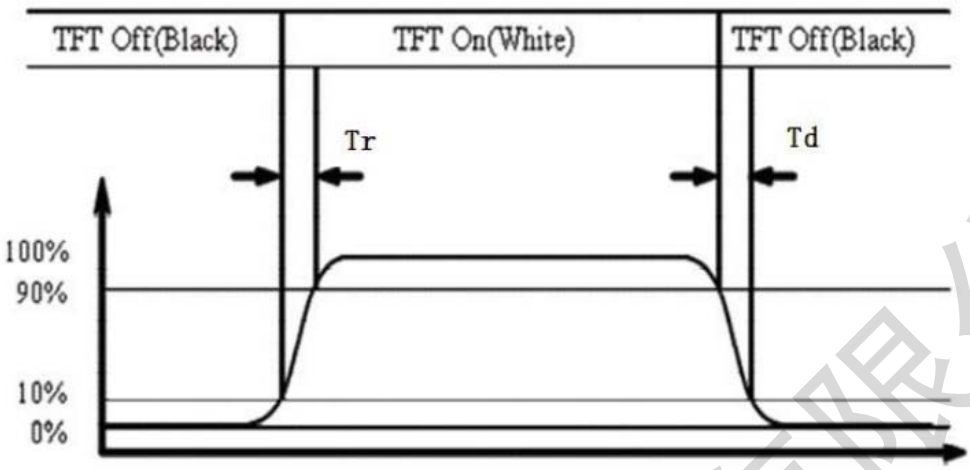


Fig. 4-3 Definition of response time

Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of color chromaticity (CIE1931)
Color coordinates measured at center point of LCD.

Note 6: All input terminals LCD panel must be ground while measuring the center area of the panel. The LED driving condition is I_{LED}=180mA.

Note 7: Definition of Luminance Uniformity
Active area is divided into 9 measuring areas (Refer to Fig. 4-4).Every measuring point is placed at the center of each measuring area.

$$Luminance\ \ Uniformity\ (Yu) = \frac{B_{min}}{B_{max}}$$

L-------Active area length W----- Active area width

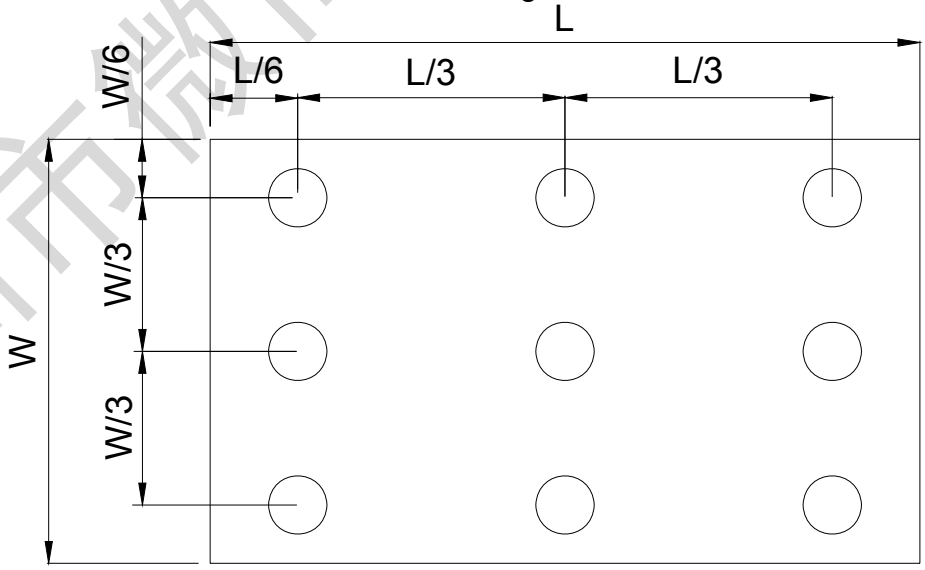


Fig. 4-4 Definition of measuring points

B_{max}: The measured maximum luminance of all measurement position.
B_{min}: The measured minimum luminance of all measurement position.